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An 8 Bit (Cascaded 4 Bits) Dual Slope ADC

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The purpose of this thesis was to create and understand the use of a dual slope ADC using Two (2) 4 Bits cascaded counters.

During the process of this thesis, both a simulation and actual laboratory works were done to compare and verify the operations as compared to the theory being investigated. The making of this Dual Slope ADC was first done by creating the various parts of operation in pieces to check they function before finally putting them all together. This design was first done with the help of MULTISM simulation tool where all the design was made and the use of Ultiboard to print out the PCB layout with the 3D view.

After the simulation was done to check for errors and it efficiency, the design was made in the Laboratory and various measurements are taken. With the help of the data collected in the Lab, one was able to determine the operation of the Dual slope ADC.

The conclusion of the study showed the efficiency of the Dual slope ADC as compared to other ADCs, most especially the Single slope ADC

Keywords	Dual slope, ADC, 8 bit, counter, cascaded 4 bit

Contents

Abbreviations

MOSFET: Metal Oxide Field Effect Transistor

PCB: Printed Circuit Board

ADC: Analog to Digital converter

DAC: Digital to Analog converter

V_{in}: Input Voltage

V_{ref}: Reference Voltage

MSB: Most Significant Bit

LSB: Least significant Bit

SNR: Signal to Noise Ratio

OPAMP: Operational Amplifier

RMS: Root Mean Square

F_{sample}: Sample Frequency

1 Introduction

1.1 Background

This thesis takes into consideration the Analog to Digital converters more especially, the Dual slope Analog to digital converter.

The purpose of this work was to understudy the functionalities as well as the operations of the various converters (AD/DA converters) with emphasis laid on the Dual Slope ADCs.

The main purpose was to construct a 16bit Dual Slope AD converter with an input voltage of 5V.

The construction of these various converters was first done using a simulation tool known as MULTISM 12.0 and this generates the expected various results required. A counter of frequency 1KHz was constructed in the simulation as it was used for the timing of the switches.

After the result is gained, the converters were then built using the Mentor graphics (Pad logic and Layout) to design the board and then the board milled with components place on it.

The final Printed Circuit Board (PCB) was then calibrated with the clocking of the switches done manually this time and the various resulted tabulated and compared to the simulated version to check for accuracy.

1.2 Relevance of the thesis topic

The Dual slope ADC is an analog-to-digital converter that does its conversion using quite low bandwidth as its input. Though the operation is quite slow, it has the ability to reject high frequency noise. It is very much useful in industrial environment that have a lot of noise by providing a good resolution when used within a fixed frequency of 50Hz and 60Hz.

The use of low current supply makes it quite adequate for use in various forms.

This technique of conversion helps do away most of the problems associated with capacitor and comparator. It also has the ability to achieve a good accuracy without having to put extreme requirements on the components stability.

Dual slope conversion is very much preferred in precise digital multi-meters, and also in 10-bit to 18-bit conversion modules.

Its ability to give a good and accurate results, high stability at the low cost, and an excellent rejection of interference (eg. power-line), for applications where speed is less required makes it quite relevant for this thesis.

1.3 Introduction to the thesis topic

There are many ways of converting Analog signals to Digital (voltage or current). But Dual slope conversion shows to be quite good when it comes to the precision resistance, eliminating noise and good stability at a low cost makes it use quite efficient and acceptable.

An input voltage which is proportional to the current (level) has to charge a capacitor for a fixed time (period) t. After it has been charged within the time interval, t, a reference voltage with an opposite polarity was applied to the integrator input when the device resets it counter. The capacitor was discharged with a constant current so that the voltage reaches "ZERO", ones the opposite polarity signal is applied. The time for the capacitor to discharge was seen to be proportional to the input voltage and this enables the counter which is also driven from a clock running at a specific frequency[6].

The Dual slope ADC seems more convenient for standard measurement in 4-digits resolution.

In this thesis, two 74LS191 ICs were used with the IRF510 MOSFETs.

2 CLASSROOM INPUT AND THEORETICAL BACKGROUND

2.1 Dual-Slope Converters

This is an approach used for very good precision low-speed analog-to-digital conversion. The input voltage signal is used to charge the capacitor so that its voltage reaches a fixed threshold. Then the digitally created circuit measures the time needed to reach its threshold by means of counting the pulses generated from a fixed-frequency clock[3,7].

This type of conversion can be used often where there is the need for high resolution but slow, low-precision converters because very little components are required.

It has two major parts: first, the circuit which digitalizes the acquired input thereby producing a pulse phase sequence and the other, the counter(N-bit) which converts the result into a digital value[1,2].

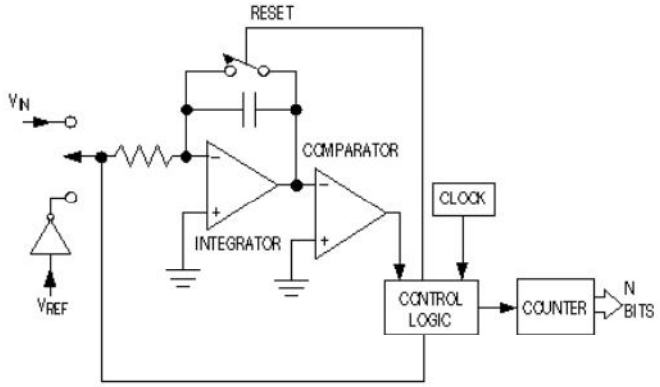

Figure 1 Dual slope setup model [1]

With this kind of conversion, there is the need for accuracy in the components measurements so as to get the precise results needed.

Working principle

The working process requires the use of the input voltage to charge the capacitor for a fixed time period. The capacitor's reference voltage discharges the capacitor and the digital control circuit measures the time for the capacitor to discharge completely. The ratio of the discharge time to the charging time is the ratio of the unknown to the known voltage[(7),3].

This conversion type operates independently of its integrator component's values, due to the fact that charging and discharging is done by the same circuit.

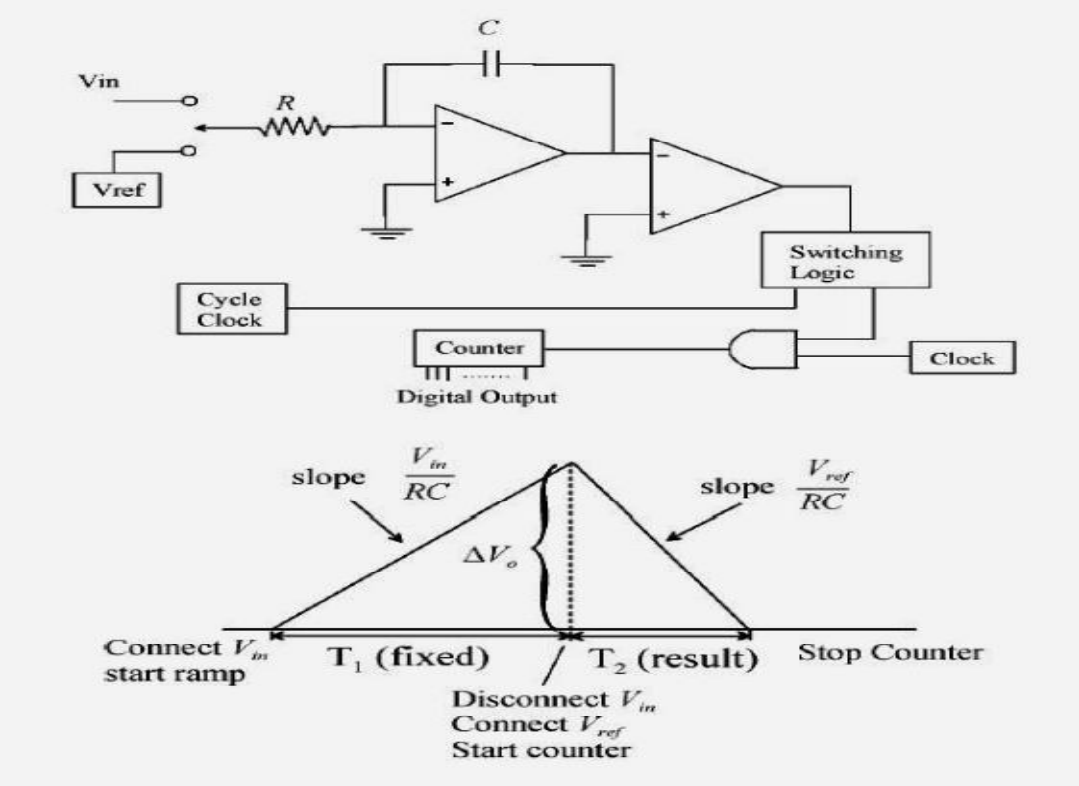

Figure 2 Dual slope conversion cycle [(7)]

The Dual slope ADC circuit, is made up of a switch, an integrator, a timer showing the needed time when the unknown voltage is integrated the unknown and measures the reference voltage timing as well as the controller, and a comparator. The switch should be placed between the voltage measured and the reference voltage (negative). Based on the kind of operation, resetting the integrator, thus by discharging is done by a parallel connection of the integrator capacitor.

This Dual slope conversion has two phases; the run-up also referred to as the 'counting up' phase and the run-down phase(counting down). During run-up, the voltage supplied to the integrator is measured. At which point, the input voltage provided to the integrator which is selected by the switch is measured. The integrator is then allowed to ramp for a fixed interval of time for the charging of the capacitor. For the run-down phase, an input to the integrator is in the form of a negative reference voltage [(1),5], the switch then chooses this

reference voltage to be its input voltage of the integrator. The time taken for the integrator's output to return to zero value is measured during this phase.

At constant input, integrator can be shown by equation 1, given as:[2]

$$V_{out} = -\frac{Vin}{RC} tint + Vint \quad \text{..... (1)}$$

If the integrator voltage initially at the beginning of each conversion is zero and that at the end of the run down period will be zero, these equations represents(equation 2 and 3) the two phases:

$$V_{out\text{-}up} = \frac{Vin}{RC} tu \quad \text{..... (2)}$$

$$V_{out\text{-}down} = -\frac{Vref}{RC} td + Vout - up = 0 \quad \text{..... (3)}$$

Solving we get:

$$V_{in} = -V_{ref}\frac{td}{tu} \quad \text{..... (4)}$$

Where V_{out} is the output voltage

V_{ref} is the reference voltage

V_{in} , the input voltage

R and C, resistor and capacitor respectively

$V_{out\text{-}up}$, output voltage during up ramp

$V_{out\text{-}down}$, output voltage during down ramp

$V_{initial}$, the initial voltage supplied

t_{int}, Initial time

t_u, time during ramp up stage

t_d, time during ramp down stage

An input signal applied to the integrator; meanwhile that same time, the counter is started. The count starts from 0 due to the comparator output counting clock pulses. Within a particular time (T) that has been assumed or pre-determined, the counter will be able to reach its maximum count, the control circuit changes by switching to an new reference voltage having an opposite polarity to the integrator input. At time T+, the charge accumulated by the integrating capacitor is proportional to the average value of the input over the interval T. The integral of the reference is an opposite-going ramp having a slope of VREF/RC[2,16]. During this period, the counter resets itself. As soon as the integrator output reaches zero, the comparator output also reaches zero and the count stops, then the capacitor voltage resets along with the switching to Vin from Vref again. The charge gained is proportional to VIN × T

The lost charge is proportional to VREF × tx,

The ratio of number of counts (no. Of counter bits set to 1) relative to the full scale count is proportional to tx / T.

The output of the counter displays number(which can Hexadecimal, octa-decimal or binary), this will be the representation of the input voltage.

This method is quite slow compared to other conversions, because sufficient conversion time is needed to count up to 2*N* by the counter. This method is much preferred for high precision converters due to the its accurate level.

Resolution of dual-slope adc

Dual-slope integrating of ADC resolution can be primarily determined by the time the clock runs up and down with the switch and the controller's clock frequency used at that moment. The required resolution (in number of bits) shows minimum length of the run-down period for a full-scale input

(*VIN* =−*Vref*) ..... (5)

$$t_d = \frac{2^r}{f_{clk}} \quad \text{..... (6)}$$

Pros of the Dual slope ADC conversion includes;

- Ability to operate on Low supply current
- High resolution
- Unique noise rejection property

The major CON for the Dual slope conversion is that it operates on a low speed, so much time is needed if there are few operations running.

2.2 AD/DA CONVERTORS

Analog to Digital Converters

An analog to digital (A/D) converter is used to performs ADC functions.

A controller is used to measure the physical quantity, for example temperature, pressure, force, etc. While a sensor, often called a transducer, is used to convert this physical quantity into an electrical signal (current or voltage). This electrical signal is then converted into a binary number so that the digital controller can use it.

2.3Comparators

This can be seen as the simplest type of Analog to digital converter. As its name indicates, a comparator compares two analog inputs (say V_{in} and V_{ref}) and outputs a logic signal which is high if V_{in} is greater than V_{ref} or low otherwise.

Comparators are available as ICs, figure 3.

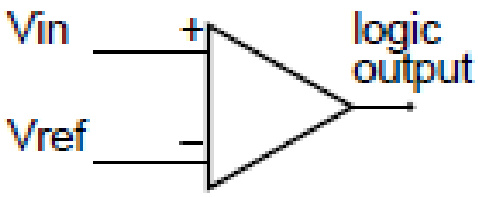

Figure 3 Operational Amplifier preferred for comparators [online]

A comparator is sometimes considered as a one-bit ADC since it has an output that compares the reference voltage and input voltage to check either one is below or above the other. Though comparators does not give too much precision, it is often sufficient since for many applications it's only necessary to determine whether some quantity is above or below some threshold[(7),2].

2.4 Sampling

Sampling is required when there are so many continuous signal in a digital system to be processed as indicated in Figure 4:

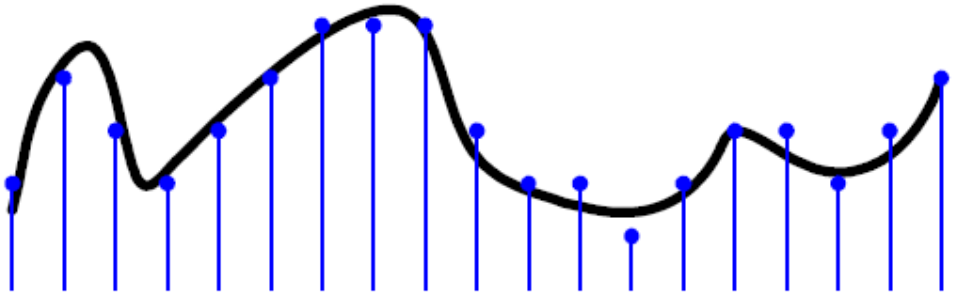

Figure 4 Sampled signal [online]

2.5 Time Quantization

Refers to the samples that are taken continuously over a particular time interval: sample frequency of f_{samp}. This causes aliasing and there is little or no information lost when the frequency containing that information is below half of the ample frequency,$½f_{samp}$. The limit for this can be referred to as the *Nyquist limit*.

Amplitude Quantization

For amplitude quantization, only one finite value from different variable of each sample is taken. It therefore add a quantized noise and a little bit of distortion for certain low amplitudes.

2.6 Quantization Noise

The output voltage$V_{OUT,}$ restricted to discrete levels so cannot follow V_{in} exactly. The error, $V_{OUT} – V_{IN}$ is the quantization noise and has an amplitude of ± ½ LSB[(7),3].

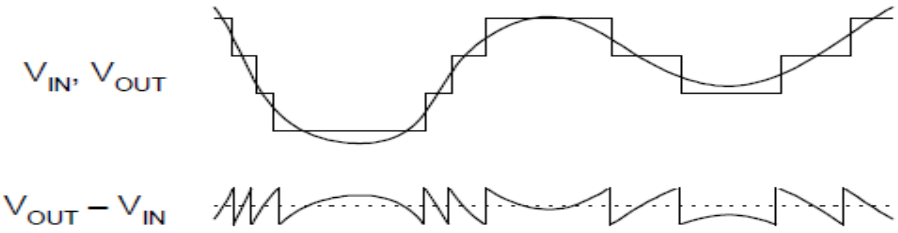

Figure 5 noise quantization[Online]

2.7 Signal-to-Noise Ratio (SNR) for an n-bit converter

This refers to the ratio of the maximum sine wave level to the noise level:

– Maximum sine wave has an amplitude of $\pm 2^{n-1}$ which equals an RMS value of[11,28]

$0.71 \times 2^{n-1} = 0.35 \times 2^{n}$. .....(7)

-SNR is:

$$20\log_{10}\left(\frac{0.35\times 2^{n}}{0.3}\right) = 20\log_{10}(1.2\times 2^{n}) = 1.8 + 6n \text{ dB}$$ ..... (8)

3 TYPES OF A/D CONVERTERS

3.1.0 Flash Converters

The Flash converter, also known as "Direct Conversion" considered one the fastest way of conversion in AD converters. ADCs based on this type of architecture are fast and can perform direct multi-bit conversion. But it requires intense analog design to manage large number of comparators that are required to build and reference voltages.

A simple way to get better (more bits of) resolution is to use more comparators. As shown below for a 2-bit flash converter we can use 2^{N-1} comparators, supplying them with reference voltages that are equally spaced over the desired conversion range. The other comparator inputs are connected to the input signal.

Figure 6.0 shows a simple direct conversion ADC with 2^{N-1} comparators connected in parallel and with N-bit resolution. Change in the input voltage results in the change in state of comparator output. Then these outputs are combined in logic circuits which produce a parallel N-bit output from the converter. Although these converters are the fastest type available, there resolution is constrained by the available die size by increasing the input capacitance and the power consumption by the large number of comparators. The presence of repetitive structure demands accurate matching between the parallel comparator sections, because any mismatch can lead to static error such as a magnified input offset voltage (or current).
The flash ADCs are prone to erratic and sporadic outputs called as “sparkle codes.” Sparkle codes have two major sources:

- Thermometer-codes bubbles.
- stability in the 2N-1 comparators

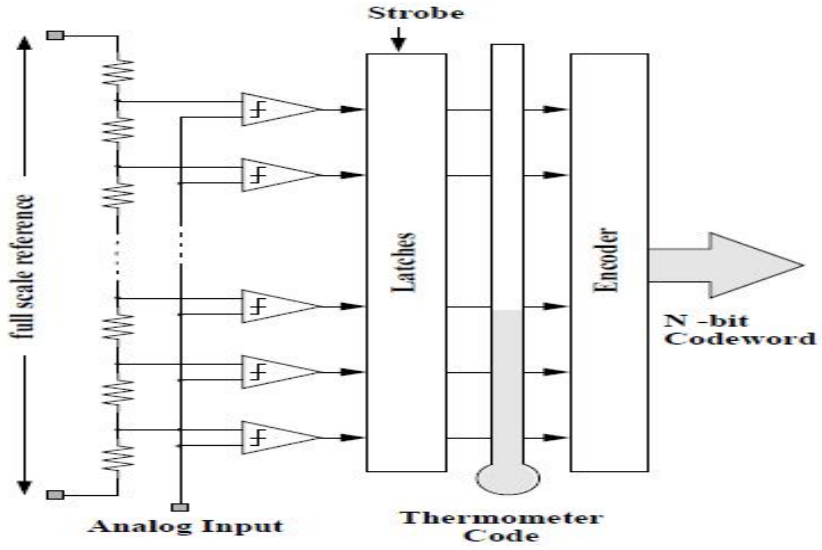

Figure 6 A flash converter [online copy]

All of the digital outputs connected to reference voltages below the input signal will be true and all of the outputs with reference signals above the input signal level will be false. The output logic circuit converts these 2^{N-1} binary values into an *N*-bit number.

Resistor chains are used to generate the threshold voltages. a priority encoder logic must determine the highest gain input that equals 1.

Example; an 8-bit converter needs 256 comparators on a single chip.

TABLE 1, illustrating an example of 8 bit converter operation

	G7:1	**X2:0**	**Example: G2 • !G4**
$V_{IN} > 1.25$:	1111111	011 =+3	0
	0111111	010 =+2	0
	0011111	001 =+1	0
	0001111	000 =+0	0
	0000011	110 =–2	1
	0000001	101 =–3	0
$V_{IN} < –1.75$:	0000000	100 =–4	0

G4 G2 .....(11)

3.1.1 Pros are

a) They are very fast

b) Also have a high input bandwidth

3.1.2 Cons

a) Consumes a lot of power

b) Have a large die size

c) Requires a very high input resistance

d) Expensive

e) Sparkle codes

3.2.0 Successive Approximation Converters

In this type of conversion (also known as bit weighing conversion), a D/A converter is used to generate a reference voltage while a comparator is later used to compare the input and voltage. A comparator that compares the voltage, a DAC, a register(successive approximation) and control logic. The D/A output can be step up by the use of a digital circuit through to a point where there is the indication by the comparator that the input signal is now lesser than the reference signal. The digital input to the D/A would correspond to the voltage step that is the next-highest to the input signal. This approach would take up to 2*N* comparisons[7,3].

Figure 7, shows the model of the successive approximation ADC

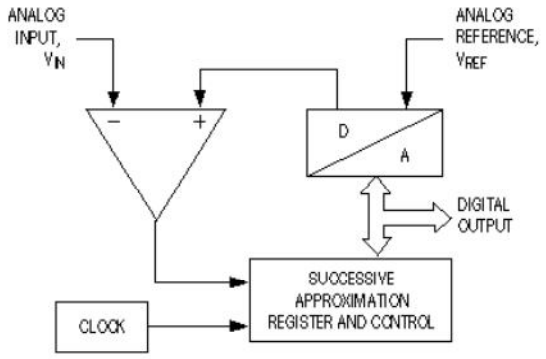

Figure 7 Successive Approximation model [3]

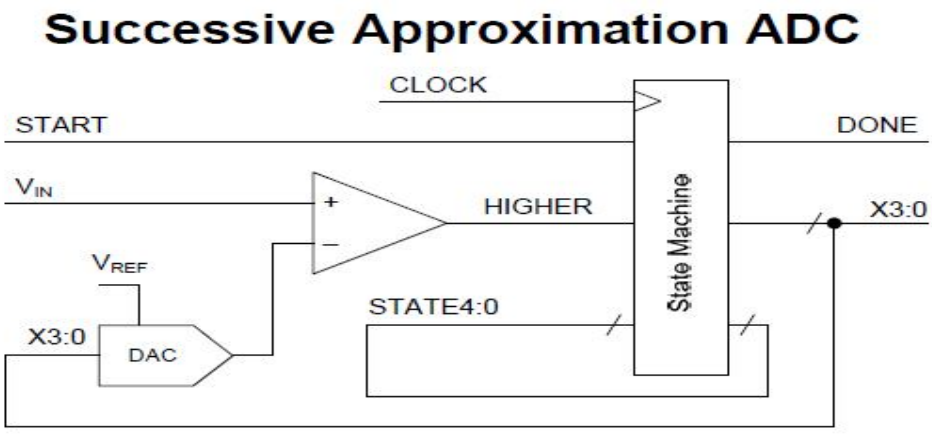

Figure 8 Operation of Successive Approximation [3]

The major advantages of the successive approximation ADC includes

- it having a low consumption rate (power)
- Ability to give a high accuracy with good resolution
- Only less external components required

While on the other hand, it poses a very limited rate when sampling, a bandwidth with a low input and inability to change the input voltage during any conversion.

3.3.0 Other types of ADC

There are other types of Analog-to-digital conversions that includes

- Binary and Gray coded ADC
- Sigma Delta ADC
- Delta encoded ADC
- Wilkinson ADC
- Etc.,

3.4 Digital to Analog Conversions

In this kind of conversion, it involves the use of a circuit, can be a chipset, to converts digital variables to analog form, i.e. voltage or current. The digital to analog converters mostly used as a control device. These can be use in to control other devices that needs a specific amount of voltage or current for their operations. These may include acoustic devices like speakers, motors with variable speed.

The most purpose of the type of conversion in the laboratory and production sectors are the creation of a required waveform.

3.5 D/A Converters

Digital to analog converters, are some kind of component converts a digital variable or data and then later converts it to its corresponding analog state(voltage or current). Its operate as the reverse of an A/D converter function does. The digital to analog converter has the capabilities of only producing a uniquely representation of an analog voltage which has been quantized, there cannot produce any output voltage with infinite range.

There are various types of DA converters, these includes

- The Resistor Ladder D/A converters
- Binary weighted D/A converters
- Delta-Sigma DAC
- Segmented DAC
- Hybrid DAC
- Pulse modulator DAC

A summary of some few of them and how they operate will be discussed below.

3.5.1 The Resistor Ladder D/A Converter

This converter type requires a precise voltage as its reference. The voltage then, has to be divided into 2^{N-1} section(as in sequence)by the use of an internal voltage divider.

N represents a specific number of bits required by the converter. Each switch turned on at a particular period corresponds to its actual dc level. Figure 9, showing a model and how each is connected.

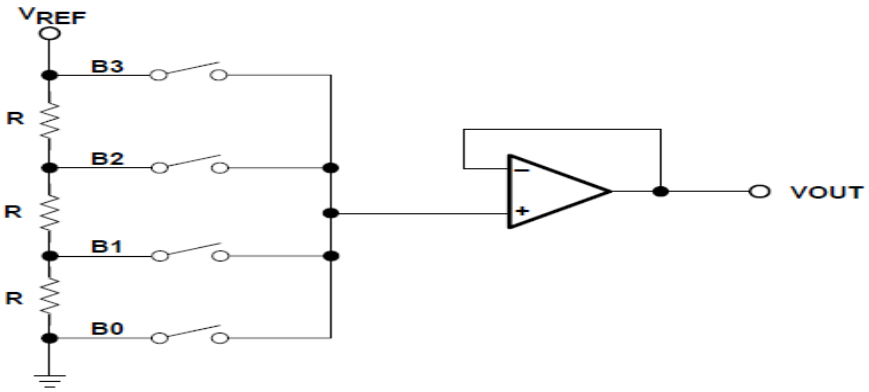

Figure 9 Resistor Ladder DA converter

The major flaw for this conversion is that, the switches and resistors has to be doubled anytime an addition is made to the resolution bits.

3.5.2 The Delta-Sigma DAC,

Considered as an oversampling DAC uses a technique where the density of the pulse is required for conversion. This technique allows the internal use of the DAC for a lower resolution .An inherently linear bit is chosen, mostly 1 Bit. A pulse density modulated signal, made by a the feedback is responsible for driving the chosen inherent linear bit. The feedback then acts as a high-pass filter for the quantization (signal processing) noise[(10)]. Due to the linearity which is high and can be made at lower cost, it makes it quite easier for most high resolution DACs (16 bits or more) to be made by this type of conversion.

Delta-sigma DACs can be used to attain an ultimate high speed per resolution(even more than 100,000 samples per second) with resolutions of about 24 Bits. Simple first order Delta-Sigma modulators or higher order topologies such as MASH - 'Multi stage' noise Shaping can be used to generate the pulse density signal. Higher oversampling rates relax the specifications of the output Low-pass filter and enable further suppression of quantization noise[(10)].

3.5.3 The Binary Weighted DAC

Consists of a resistor per bit or current source per bit of the DAC, which links up to a summing point[(10)]. A required output voltage is summed up by this precise voltages/current. This can be regarded as one of the fastest conversion types though it has flaw of poor accuracy due of the high precision required for each individual voltage or current. Such high-precision resistors and current-sources are expensive, so this type of converter is usually limited to 8-bit resolution or less[(10)].

4 METHODOLOGY

The experiment was carefully performed in batches by breaking them in to various part in order to understand the how those sections work and its corresponding output before connecting or merging the various sections to attain the complete circuit.
These sections are

- The switch
- The integrator
- 16 BIT counter (TWO cascaded 4BIT counters)
- Flip flop

4.1 The switch

The switch in a dual slope ADC is made of Two IRF510 MOSFET (which is an N-Channel enhancement) was used to make the switch with one of them being inverted to serve as P-Channel. A dual switch is connected to the 5V Vcc power source and a ground, so that it would be alternated between those two (2). The switch was then connected to the MOSFET (IRF510) through the Gate, creating an N-channel and another connected via an inverted to the other MOSFET thereby creating a P-Channel. The P-channel side of the switch was passed through a comparator to stabilize and get rid of unwanted signal (noise) and then the output connected back to the N-Channel which was then passed through another comparator.

4.2 Comparator

The comparator, figure 10, which comprises of the OPAMP as well as its other components (resistors,..) with the calculated or required values obtained through its calculations. This comparator takes the output feed from the switch and eliminate any noise from and then the output fed to the Integrator.

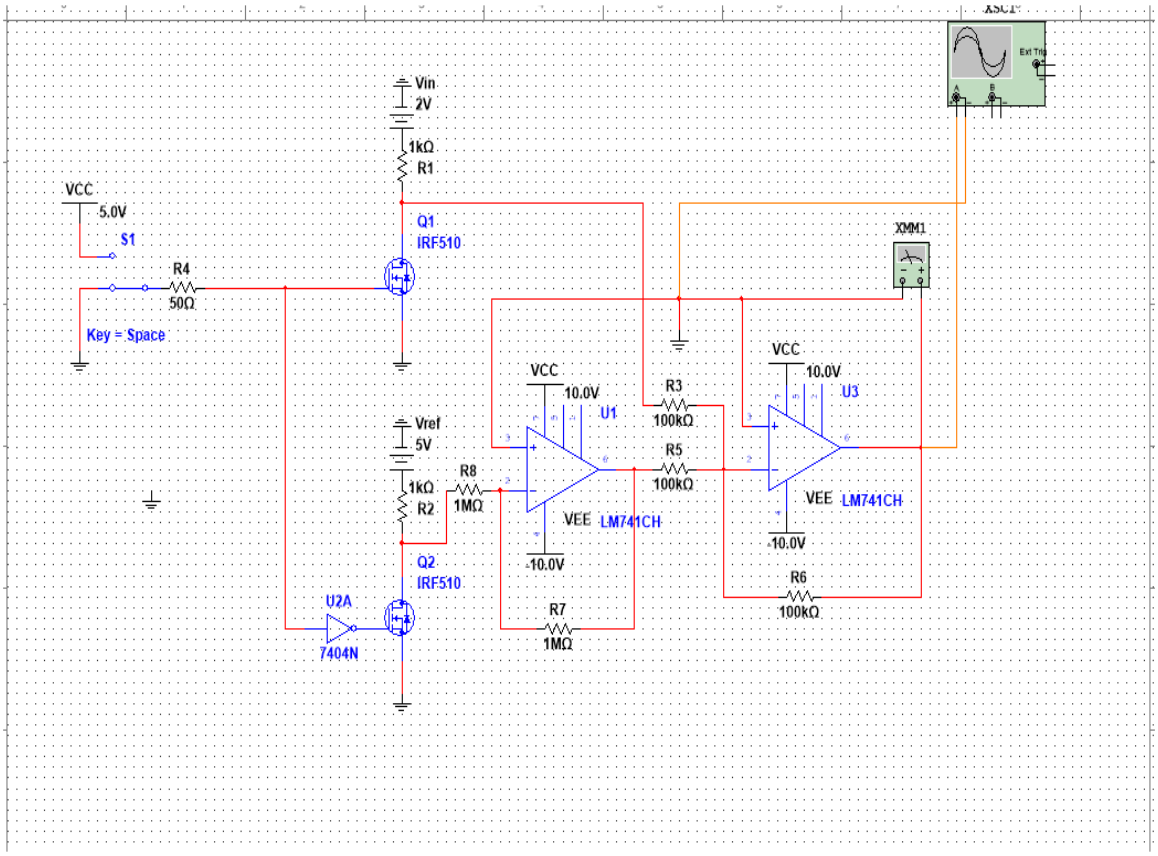

Figure 10, the IRF510 MOSFET switch from multisim simulation

4.3 Integrator

The output from the switch was received at the input of the Integrator, which was mainly a current. This current which is proportional to the input level charges the capacitor for a fixed time period and the capacitor is discharged by a constant current until the voltage reaches Zero again. The time required to discharge the capacitor is directly proportional to the input level and it is used to enable the counter driven by the clock running at a fixed frequency [13,6.74]. Figure 11, shows its design below

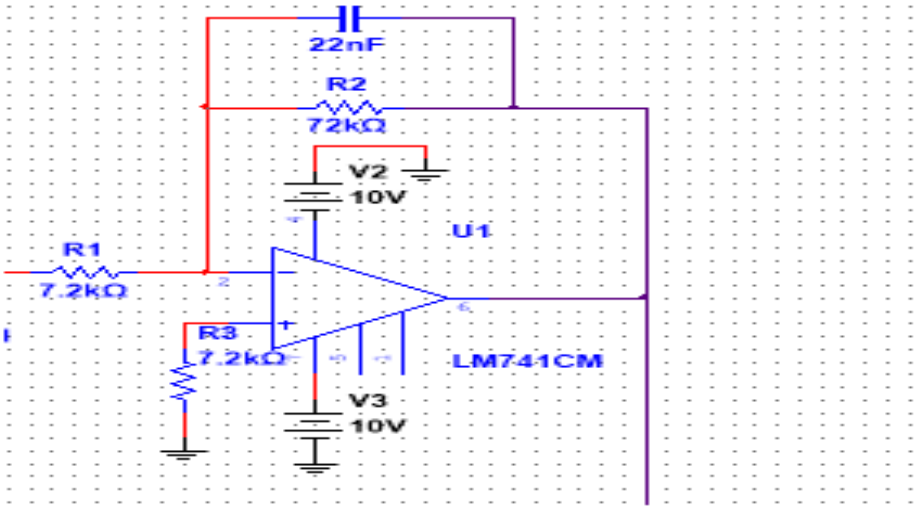

Figure 11, The integrator from the circuit(multisim)

4.4 The counter (clock)

The counter, figure 12, is a cascaded TWO 4 bit counters (making a 16 bit counter) with an LED display. This is driven from a clock which runs at a fixed frequency. The counts resets once the capacitor charges and discharges [6,634]. Then, the JK_flip flop in there resets the whole thing and feeds it back the switch for the whole cycle to begin again.

The clock frequency does not necessarily have to have a high stability [5] , because the fixed integration time during the FIRST phase of the measurement is generated by subdivision from the same clock used in the increment.

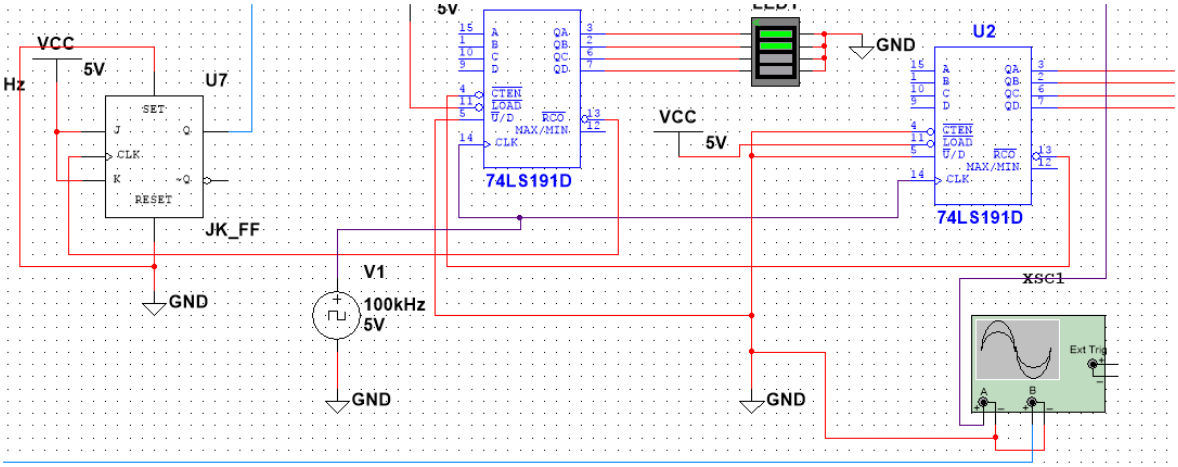

Figure 12, The two 4 BIT cascaded counter

4.5 The complete Dual slope ADC

After the various parts were tested and well simulated using the Multisim simulation tool, the various parts were brought together and the final project was completed on the Multisim tool and also verified that they worked. Figure 13, shows the complete design simulation model.

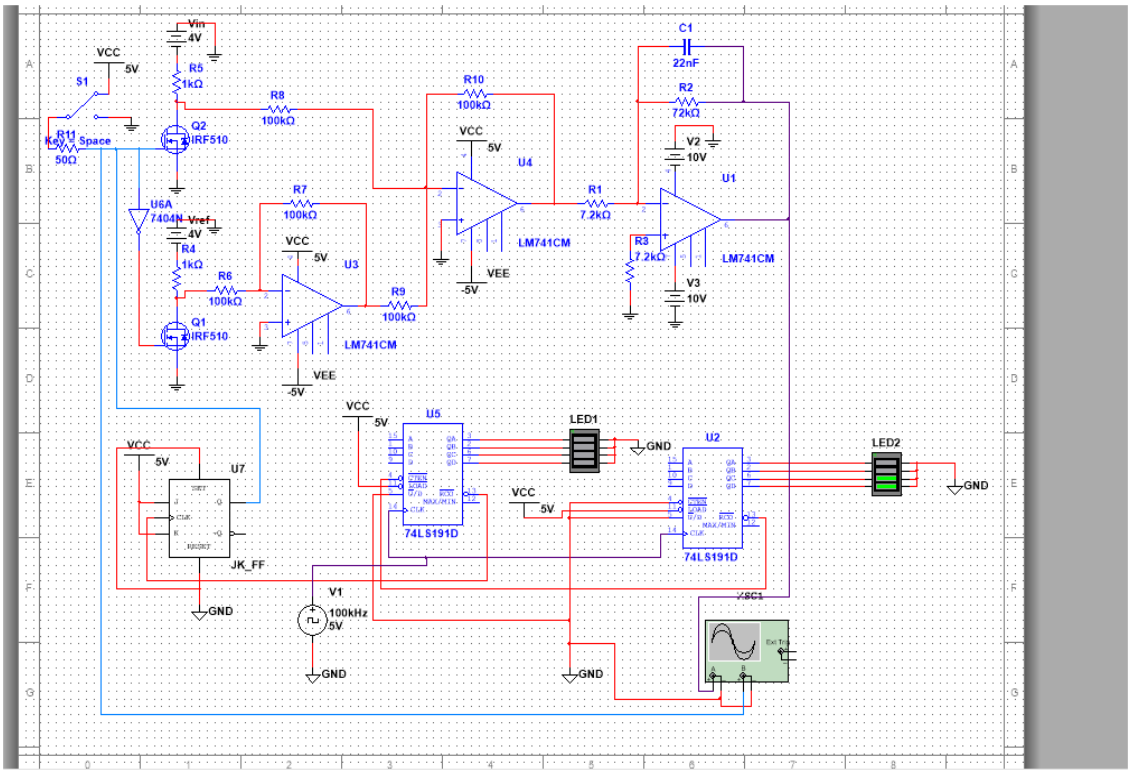

Figure 13, The complete Multisim design for Dual slope ADC

5 EQUIPMENT

In the study, some various components and equipment were used in implementing both laboratory work and simulation. This chapter will get into specifics, as well as highlighting the apparatus' relevance to the data collection.

The equipments used for the work in this thesis includes

- IRF510 MOSFET
- LM741CH
- 74LS191D
- 7404N

5.1 IRF510 MOSFET

This is an enhancement kind of MOSFET, which provides a combination of fast switching, low on-resistance and cost effective. This MOSFETS, Figure14 has a dynamic dv/dt rating , so it is much preferred and easier to use.
The TO-220 package is universally preferred for all commercial-industrial application at power dissipation levels of about 50 watts [15]. Its main properties that make it a unique choice are

- Repetitive Avalanche Rating
- Operates up to 175^0C
- Fast switching
- Ease on Paralleling
- Requires simple drive,

Table 2, indicates all the basic parameters for the MOSFET and properties

Figure 14. IRF510 MOSFET, TO-220

Table 2. PARAMETERS OF IRF510.[14]

PARAMETER	RATINGS
MOSFET TYPE	N-Channel enhancement
V_{GS} (Gate to Source voltage)	-/+ 20V
$V_{GS(Th)}$, Gate Threshold Voltage	2.0-4.0 V(V_{DS}=V_{GS}, I_D= 3.4A)
Dv/dt(Peak Diode recovery)	5.5V/ns
$V_{DS(Br)}$ Drain to source breakdown V	100V, V_{GS}=0V, I_D= 250uA
OPERATING TEMPERATURE	-55^{o}C - 175^{o}C

5.2 LM741

The LM741, Figure 15, are series of operational amplifiers are the most common and general-purpose(all purpose) OPAMP. This amplifier offers many features which makes it very user friendly in the laboratory. It also has some unique features that also helps with the usage. These includes

- An overload protection on the input and output
- No latch-up when the common-mode range is exceeded
- Has the freedom from oscillation
- Has a large working temperature range(-55^{0}C - +125^{0}C)

Table 3, shows all the basic parameters and major properties of the LM741

These unique features makes it possible to be used in various ways that includes In

- Comparators
- Multivibrators
- DC Amplifiers
- Summing Amplifiers
- Integrators and Differentiators
- Active filter

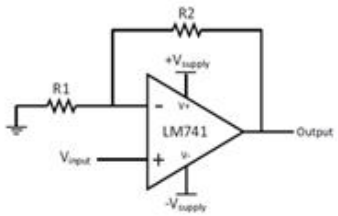

Figure 15, LM74

Table 3. PARAMETER RATINGS OF LM741

	RATING
POWER DISSIPATION	500mW
INPUT VOLTAGE	-/+15V
TEMPERATURE OPERATION	-50^0C - $+125^0$C
SUPPLY VOLTAGE	-/+ 22V

5.3 74LS191 4 BIT COUNTER(DATA SHEET, MOTOROLA LITERATURE DISTRIBUTION)

The SN74LS191,Figure 16, is a synchronous UP/DOWN Modulo-16 binary counter. Its state changes with the synchronization of the LOW-to-HIGH transition of the Clock Pulse input.

Each functions are such that, each circuit contains four(4) master/slave flip-flops with internal gating and steering logic to provide the counts(up/down) and an individual preset. Table 4, shows all other parameters for the counter.[16]

It has these features that made it quite right for its use in the making of this thesis, these includes

- Synchronize counting
- Individual Preset Inputs
- Cascade-able
- Count enable with Up/Down inputs
- Low power Dissipation(90mW0
- High speed frequency count

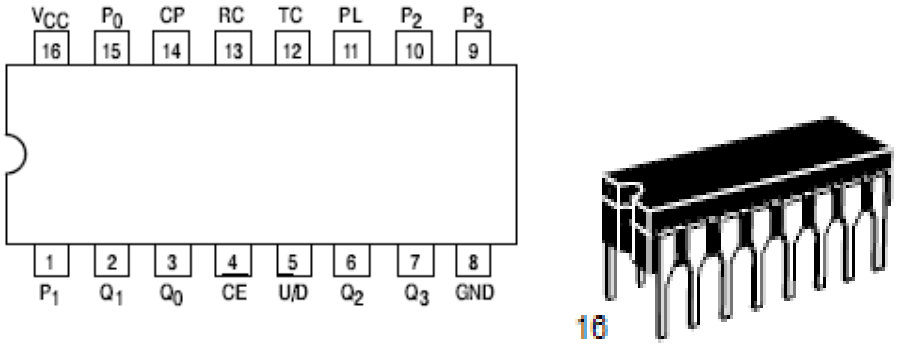

Figure 16, SN74LS191 showing all PINS and function

Table 4. PROPERTIES OF SN74LS191 USED [16]

PARAMETER	
VCC	4.75-5.25V
BITS	4
VOLTAGE(Normal)	5V
Max. Frequency(normal V)	25MHz

5.4 SN7404 inverter

This is an Inverter type used in making the Switch, by inverting the Positive voltage into a Negative one. This device contains Six(6) independent inverters that can operate or can be used differently at the same time. It has a quite good operational temperature range as well as a very high temperature storage Range[17] as shown in the Table 5 with all other parameters

Table 5. PROPERTIES OF SN7404 USED[18]

PARAMETER MAXIMUM RATING	
Supply Voltage	4.75-5.25V
Operating temperature	0 C to +70 C
Propagation delay time	22ns
Storage Temperature Range	-65^0C to $+150^0$

6 Measurements And Analysis

6.1 Counter

This chapter takes into account the values(data) obtained from the Laboratory as well as the simulation diagrams related to the topic of the thesis. It mainly contains the outcome of the thesis(Results), the spectrum analyzer figure and data used to compare the actual laboratory work to the theoretical aspect.

Firstly, the Cascaded 4 Bit counters were constructed by using the Multisim simulation tool. This was allowed to run all of its 16 Bits course to verify there were no errors in the counter. As the counter was done and its simulation completed, it was observed that the 74LS191 had been accurately calibrated and therefore NO error was found throughout its counting.

As shown in Figure 17 and 18, the 74LS191 was connected to an External display to show the count in real numbers to confirm the actual count before it was then used in the making of the topic of the thesis.

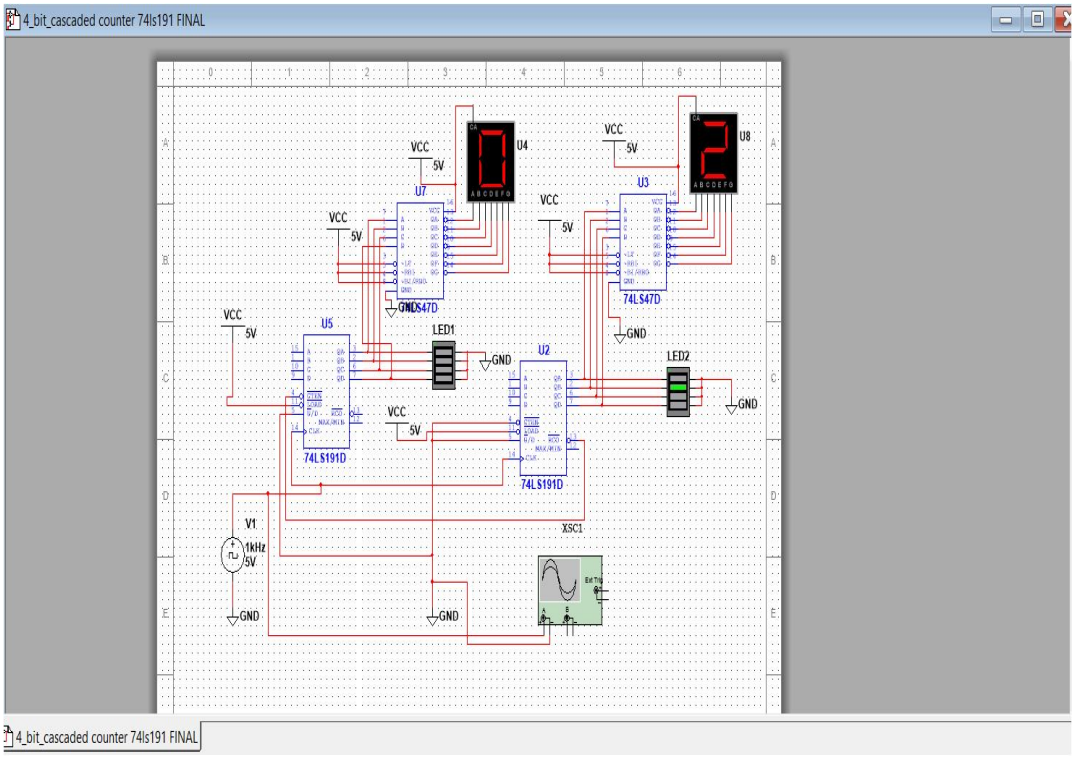

Figure 17, The result shown by the Cascaded 4 Bits(8 Bits) counter at START

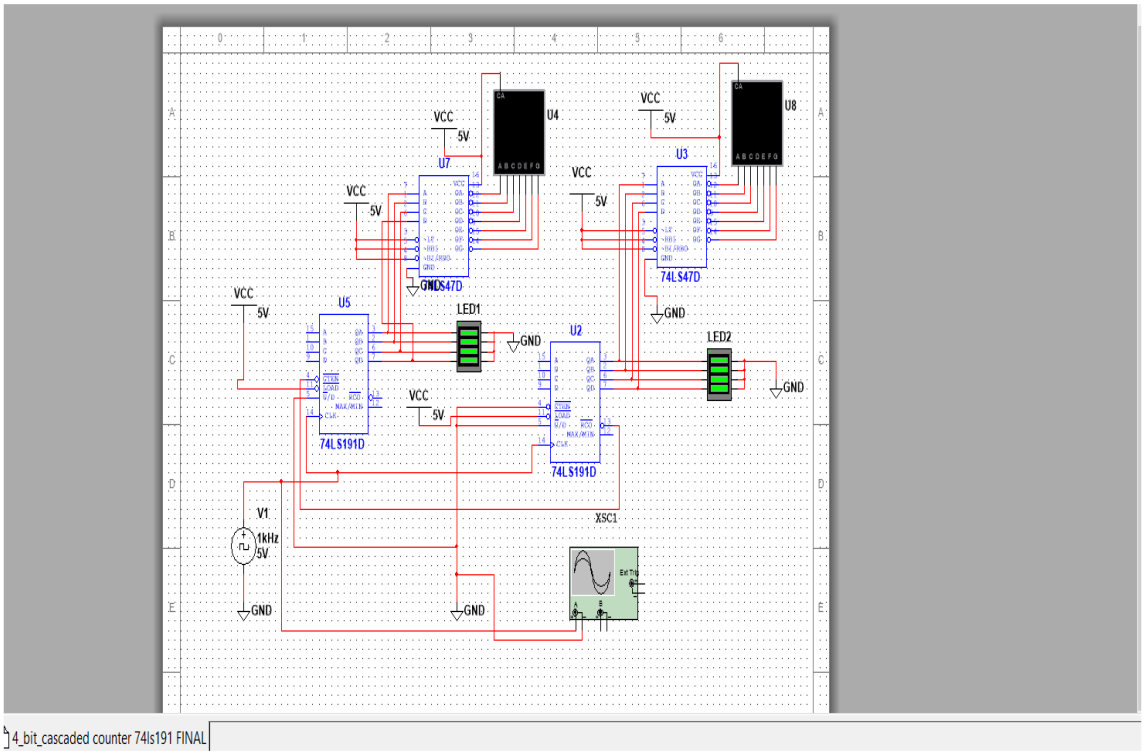

Figure 18, Result shown by the counter at FULL count

This design was made with 5V source(Vcc) and was controlled by the Clock voltage with a set Frequency of 1Khz and 5V voltage supply.

6.2 The switch

The switch for the Dual Slope ADC was also made separately to check for all the functionality to work before been connected to the main circuit. The switch which is made up of the IRF510 MOSFETs(two of them). With both of them been an N type enhancement transistors, one of them had to be inverted to obtain a reverse of its polarity(P type).

So an inverter(7404N) was used for the purpose.

Figure 19, below shows how the switch was tested before its inclusion to the main circuit for the thesis

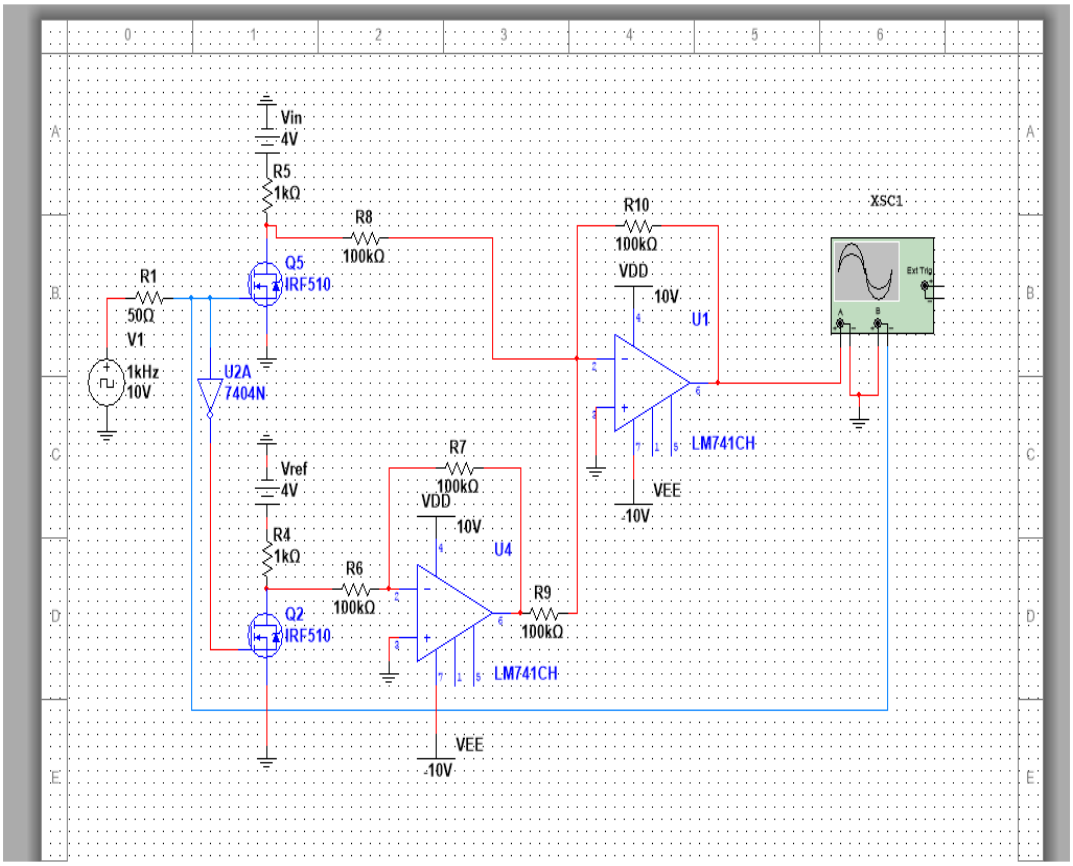

Figure 19, The MOSFET switch

6.3 J_K Flip flop

This J_K flip flop served a useful purpose in the final circuit board. Its main role in the final circuit board was to RESET the whole counter ones the count has reached its FULL potential. The reset changes the flow of the current form the its previous polarity to the opposite polarity and vice versa, thereby allowing the circuit to continue running without any break.

Figure 20, show the connection of the J_K flip flop to the counter and back to the main switch for the operations

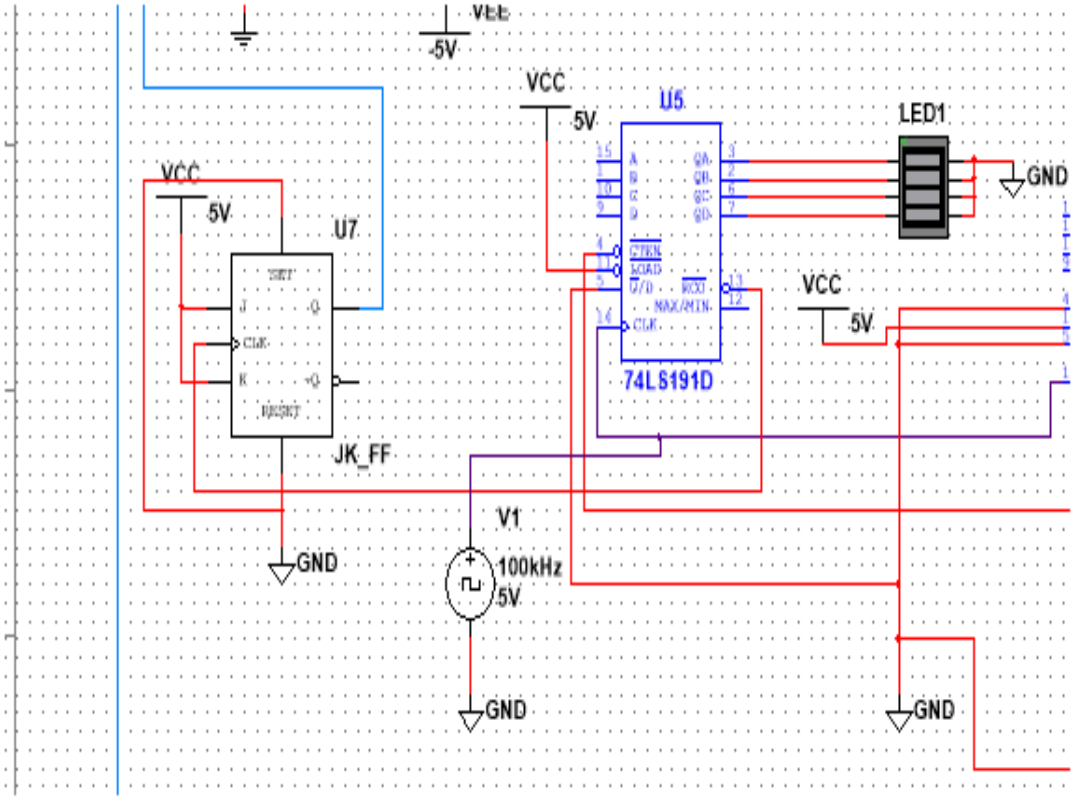

Figure 20, showing the J_K flip flop to the counter

6.4 The complete circuit

This complete circuit for the thesis shows the whole work after all the major parts put together and other part that were used to test the smaller parts eliminated from the final part of the work. The final circuit was checked for all components used and its efficiency compared to the theoretical part was very much analyzed.

This final part(complete circuit) was tested manually in the Laboratory to ensure that the operations and its analyses on from the theory matches the one in the thesis.

Figure 21, shows the Final circuit board in Multisim design board and the function generator obtain from the same program.

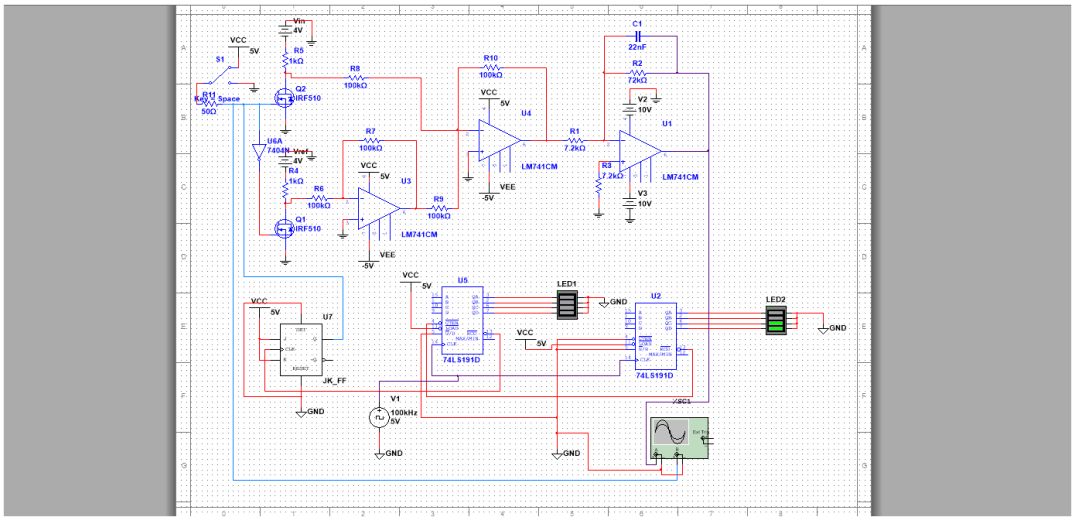

Figure 21, the complete Dual slope ADC circuit on multisim

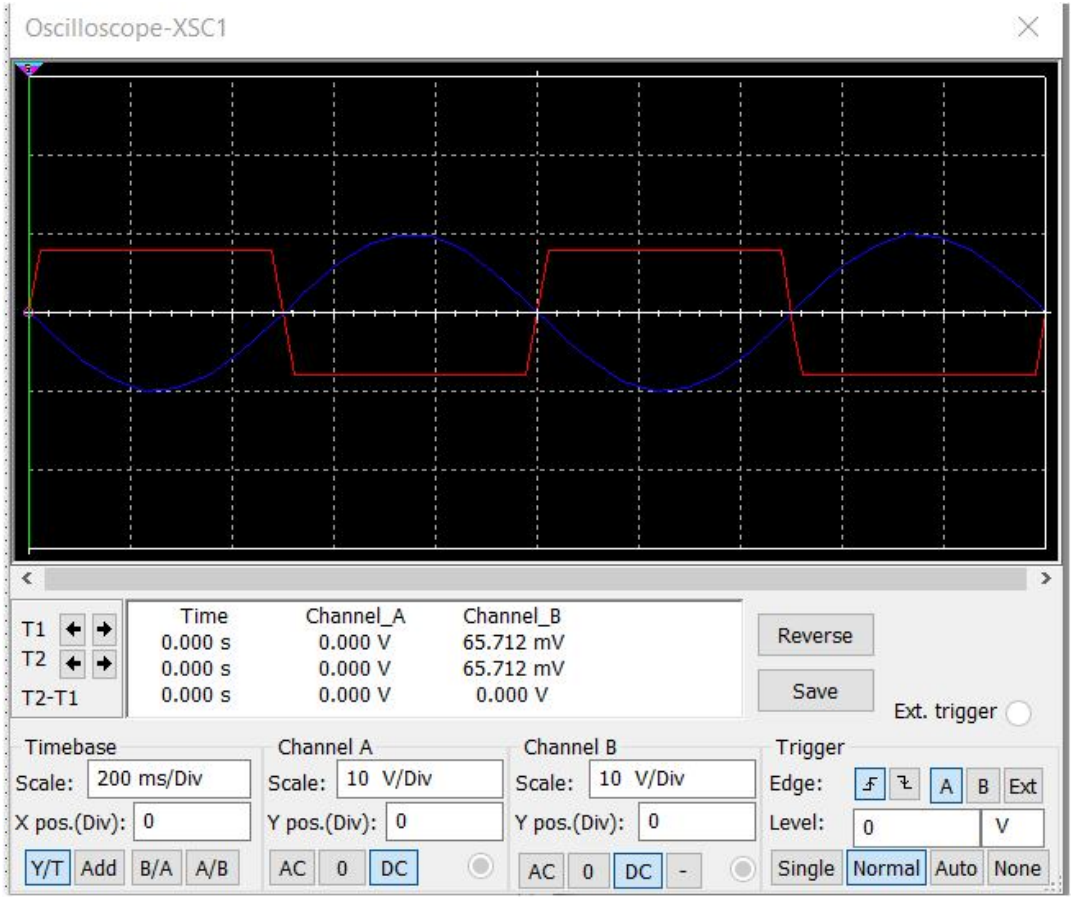

Figure 22, Oscilloscope illustration of the dual slope ADC

6.5 Circuit layout and a 3D representation using ultiboard

The complete circuit after all the connections, simulations and the measurement of the setup(Appendix 1 and 2).

The layout of the circuit was done using Multisim Ultiboard. This gives a virtual PCB(Printed Circuit Board), where the copper cables are shown, both the top and bottom layer. The connection of the wires was made manually as to the best it can be.

Figure 23, which shows the copper wiring of the final dual slope ADC circuit has all components labeled by their respective variables as seen in the Multisim full circuit in figure 21. This shows where the exact component can be found and traced back to the main circuit logic and layout at any given time.

The copper wiring of this Circuit has two colors(red, which is the Bottom layer of the PCB and green, the top layer of the PCB)

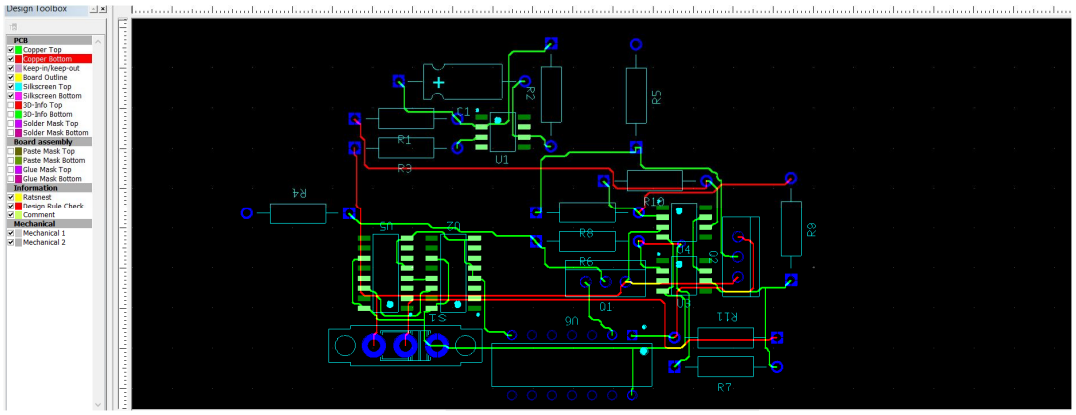

Figure 23, The layout of the Dual slope ADC

Also, after the experiment had been done, a virtual 3D representation of how all the actual components of the circuit board can be seen when they are placed on the PCB.

This gives a detail and vivid demonstration of how the components should be placed and also a real picture of each of the layers and how they corresponds to each other in the layout. figure 24 and 25 shows the copper board indicating both the top and bottom side of the board.

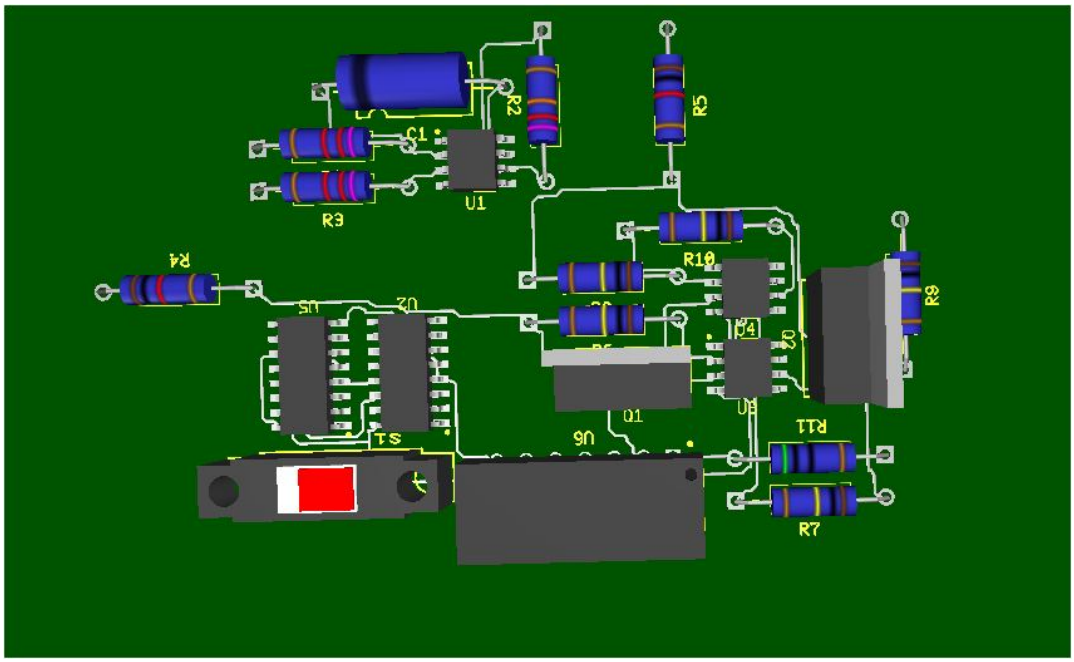

Figure 24, the top layer/ part of the circuit board

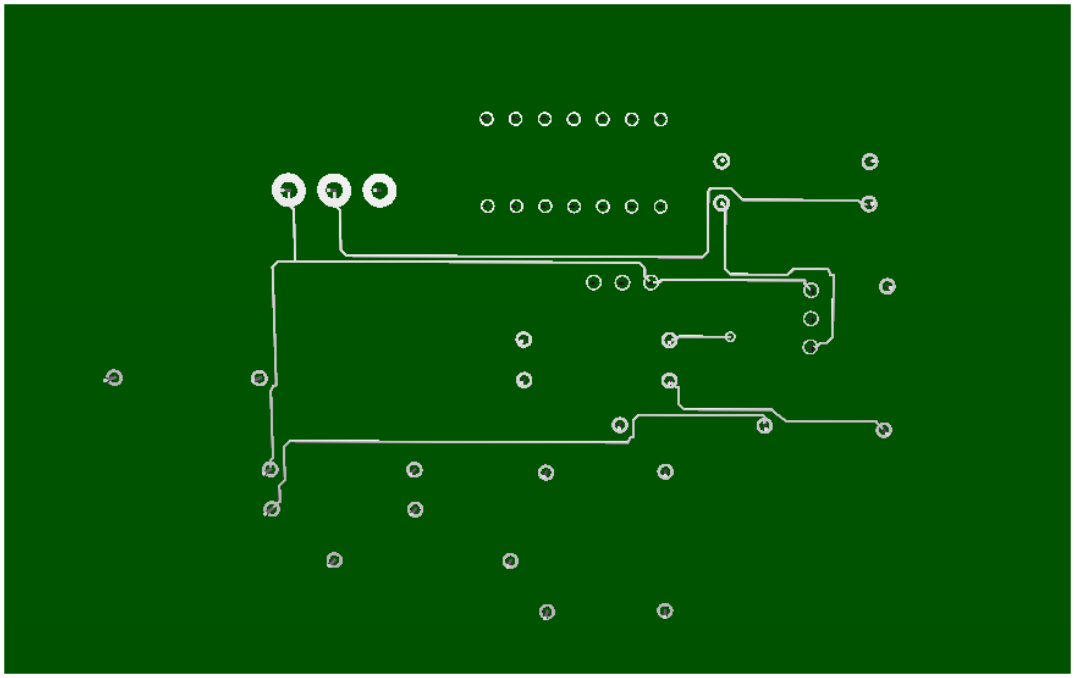

Figure 25, Bottom layer of the PCB

7 Conclusion

The main goal of the thesis was to create and study the operations of a Dual slope ADC with a 16 Bit counter (cascaded 4 Bit counter) and compare the one obtained from the study to the theoretical aspect of that ADC model.
With this design model, a comparator, integrator, switch and the cascaded counter was the major equipment required to achieved this goal.

Though, after carefully calculating the adequate values for the Resistance and capacitor needed most especially for the integrator, the actual value was not available in the Laboratory but a similar or one closer to the value was used as a replacement for the setup.

The simulation of the final work was done with the aid of Multisim, which gave a good response to the waveform expected as to that of the theory.

The actual laboratory work was carried out on a white board (in the lab), where the components were placed on the board and the function generator used to tune for the accurate frequency that is required for the waveform to form.

After the experiment, it can be concluded that a vivid and thorough work was done to verify the Dual slope ADC operations, which with the help of the capacitor which charges and discharges to set the rise and fall of the voltage level which drives the counter

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FUNCTION GENERATOR

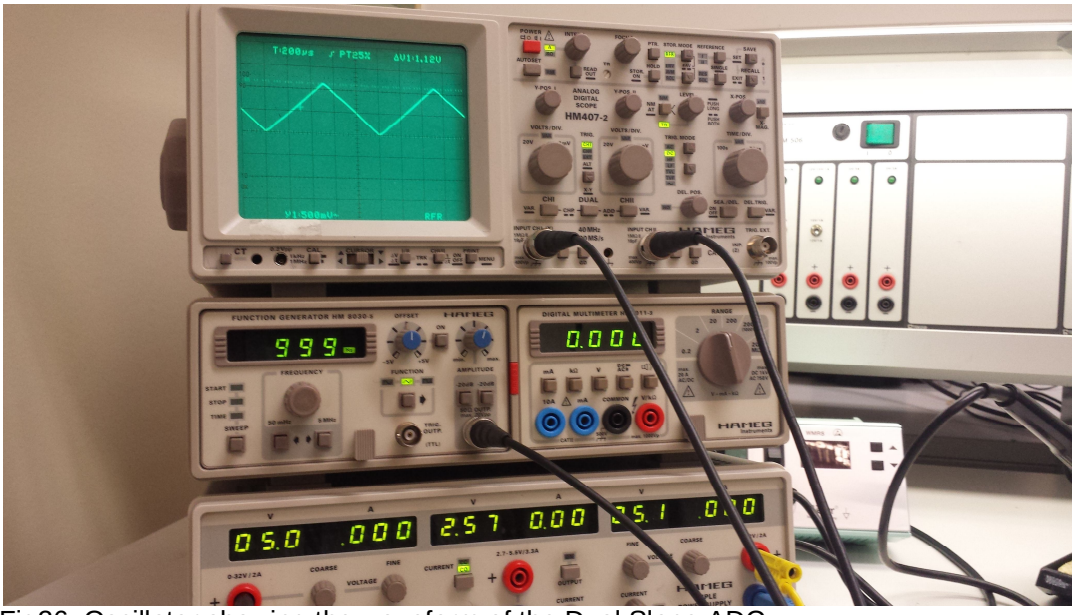

Fig26: Oscillator showing the waveform of the Dual Slope ADC

Lab Setup

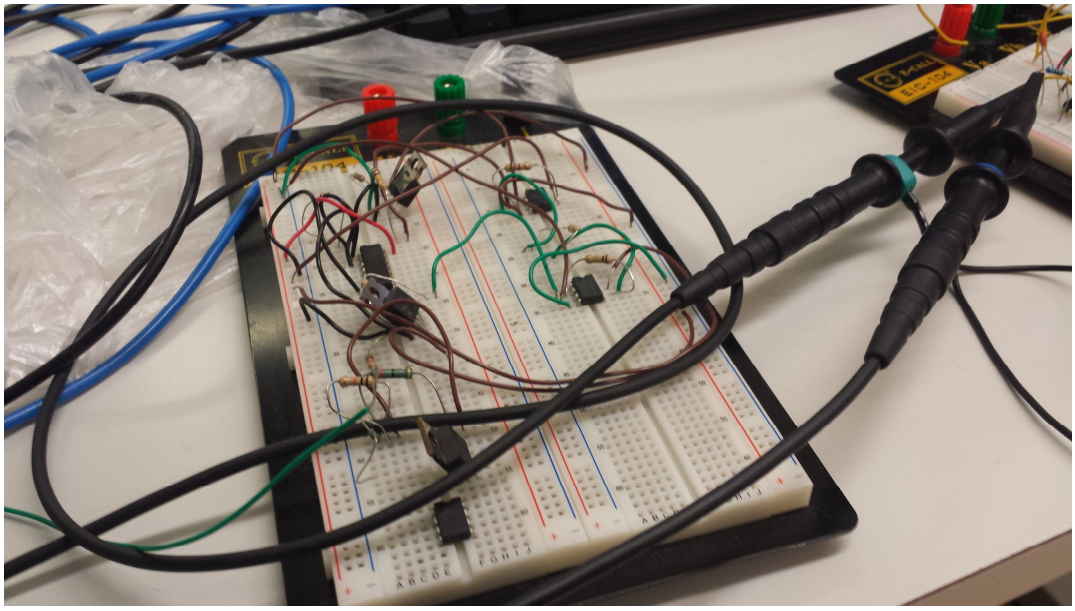

Fig29: Setup of the lab

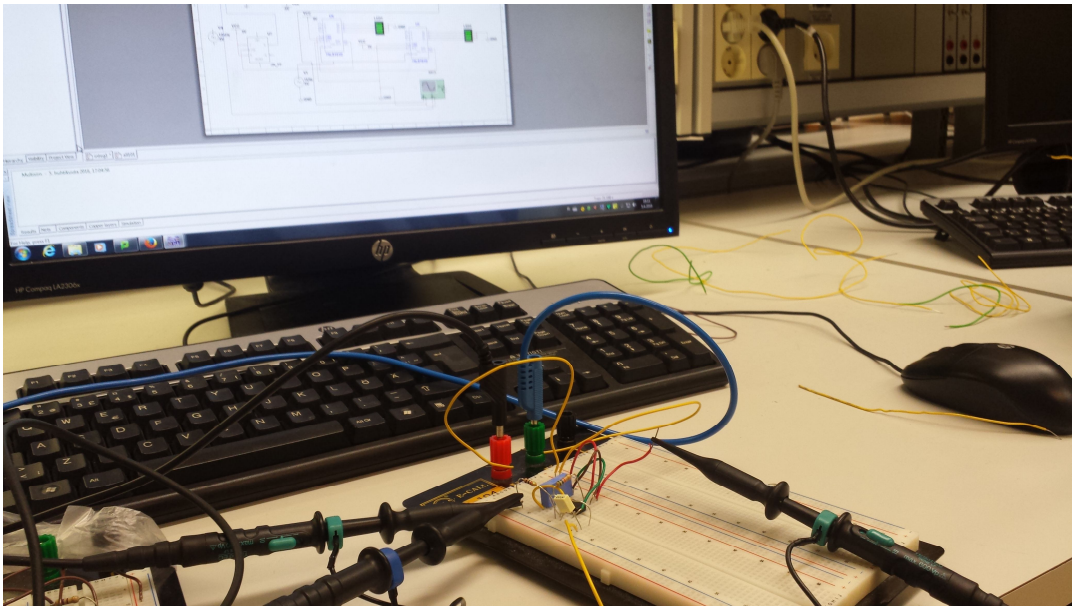

Fig 27: Setup of the lab